Department of Information and Communication Systems and Software Engineering

Verification of hardware and software designs using Model Checkers

Duration: 3 months

Supervisor: Ass. Professor Ekaterina Khvorostukhina

Ekaterina Khvorostukhina defended her Ph.D. thesis in 2011. Her research interests are in graph theory, automata theory, and mathematical logic.

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Language: English

Audience: Undergraduate or Postgraduate Students with basic knowledge of mathematical logic and skills in software development.

Learning topics

Model Checking (**a method for checking**)

Linear temporal logic, or LTL (a modal temporal logic with modalities referring to time)

Model checking tool (tool for verifying the correctness of software models in mostly automated fashion)

Learning technologies

Model-checking tools (SPIN, or PAT, or similar)

Brief description of the internship

In computer science, model checking is an efficient formal method for the verification of models. During the internship, students will gain skills in models building and their verification using model-checking tools.

An important class of model-checking methods has been developed for checking models of hardware and software designs where the specification is given by a temporal logic formula. Temporal logic is a system of rules and symbolism for representing propositions qualified in terms of time. Temporal logic has found an important application in formal verification. Therefore, students will also learn the basics of linear temporal logic during the internship.